We claim:

1. A partitionable system, comprising:

a first domain, comprising a first processor, a first firmware program, and a first interrupt table;

a second domain, comprising a second processor, a second firmware program, and a second interrupt table;

wherein the system is partitionable into the first domain and the second domain; and

a plurality of input/output devices, comprising a first single-instance device, a second single-instance device, a first multi-instance device, and a second multi-instance device;

wherein the first firmware program initializes the first interrupt table for the first single-instance and the first multi-instance devices and the second firmware program initializes the second interrupt table for the second single-instance and the second multi-instance devices when the system is partitioned into the first and second domains.

2. The partitionable system of claim 1, wherein the first processor is interrupted by the first single-instance and the first multi-instance devices and the second processor is interrupted by the second single-instance and the second multi-instance devices.

3. The partitionable system of claim 2, wherein a first operating system is booted in the first domain and a second operating system is booted in the second domain when the system is partitioned.

4. The partitionable system of claim 3, wherein the first operating system is a legacy operating system.

5. The partitionable system of claim 3, wherein the first firmware program initializes the first interrupt table for the first single-instance, the first multi-instance, and the second multi-instance devices when the system is unpartitioned.

6. The partitionable system of claim 5, wherein the first processor is interrupted by the first single-instance, the first multi-instance, or the second multi-instance devices.

7. The partitionable system of claim 6, wherein the second processor is interrupted by the first single-instance, the first multi-instance, or the second multi-instance devices.

8. The partitionable system of claim 5, wherein the second single-instance devices are unused.

9. The partitionable system of claim 5, further comprising:

a first bit to indicate that the first domain is to be cojoined with the second domain; and

a second bit to indicate that the second domain is to be cojoined with the first domain;

wherein the partitionable system is returned to an unpartitioned state when the first bit and the second bit are set.

10. The partitionable system of claim 1, further comprising:

an interrupt controller accessible to the first domain and to the second domain, the interrupt controller comprising:

a first interrupting device for sending a first processor interrupt to the first processor, the first processor interrupt coming from either the first single-instance device or the first multi-instance device;

a second interrupting device for producing a second processor interrupt to the second processor, the second processor interrupt coming from either the second single-instance device or the second multi-instance device; and

wherein the first interrupting device receives both the first processor interrupt and the second processor interrupt when the system is partitioned.

11. The partitionable system of claim 10, wherein the first interrupting device receives the first processor interrupt and the second interrupting device receives the second processor interrupt when the system is not partitioned.

12. The partitionable system of claim 10, further comprising:

a two-input multiplexer for routing interrupts from either the first interrupting device or the second interrupting device to the second processor.

13. The partitionable system of claim 12, wherein the two-input multiplexer routes interrupts from the first interrupting device to the second processor when the system is not partitioned and routes interrupts from the second interrupting device to the second processor when the system is partitioned.

14. The partitionable system of claim 1, further comprising a first reset handler, wherein the first reset handler issues a hard reset to all processors and all input/output devices when the system is not partitioned.

15. The partitionable system of claim 14, further comprising a second reset handler, wherein the first reset handler issues a second hard reset to the first processor, the first single-instance device and the first multi-instance device while the second reset handler issues a third hard reset to the second processor, the second single-instance device and the second multi-instance device when the system is partitioned into the first and second domains.

16. The partitionable system of claim 14, wherein the first reset handler issues a power good reset to all processors and input/output devices whether the system is partitioned or not.

17. A partitionable system, comprising:

a first connector coupled to a bus; and

a second connector coupled to the bus, the second connector coupling the partitionable system to a chassis by a cable;

a first controller coupled to the bus, wherein the first controller transmits an identification signal to the first connector; and

a second controller coupled to the bus, wherein the second controller transmits a second identification signal to the second connector when the system is partitioned, but the first controller transmits the second identification signal to the second connector when the system is not partitioned.

18. The partitionable system of claim 17, further comprising a chassis coupled directly to the first connector, the chassis comprising a third controller, a third connector, and a cable coupling the first connector to the third connector, wherein the third controller in the chassis detects the identification signal.

19. The partitionable system of claim 18, wherein the chassis comprises a fourth connector for coupling to a second chassis, the second chassis comprising a fourth controller and a second cable, the second cable coupling the fourth connector to the third connector, wherein the fourth controller in the second chassis does not detect the identification signal.

20. The partitionable system of claim 19, wherein the fourth controller in the second chassis can obtain the identification signal by querying the third controller.

21. The partitionable system of claim 19, wherein the first controller sends non-identification signals to the first connector and the fourth controller in the second chassis detects the non-identification signal.

22. A method, comprising:

identifying input/output devices in a system, the input/output devices comprising first single-instance devices, first multi-instance devices, second single-instance devices, and second multi-instance devices;

determining that the system is to be partitioned; and

initializing an interrupt controller such that the first single-instance and first multi-instance devices interrupt a first processor in a first domain while the second single-instance and second multi-instance devices interrupt a second processor in a second domain.

23. The method of claim 22, further comprising:

configuring a first interrupt table to receive interrupts from the first single-instance and first multi-instance devices.

24. The method of claim 23, further comprising:

configuring a second interrupt table to receive interrupts from the second single-instance and second multi-instance devices.

25. The method of claim 24, further comprising:

determining that the system is not to be partitioned; and

initializing the interrupt controller such that the first single instance devices, the first multi-instance devices, and the second multi-instance devices interrupt both the first processor and the second processor.

26. A system, comprising:

a first connection between a first reset handler and a first domain, the first domain comprising one or more processors and input/output devices, wherein the first reset handler produces a first hard reset signal;

a second connection between a second reset handler and a second domain, the second domain comprising one or more processors and input/output devices, wherein the second reset handler produces a second hard reset signal; and

a multiplexer, wherein the first hard reset signal and the second hard reset signal are received as inputs to the multiplexer;

wherein the multiplexer sends the second hard reset signal to the second domain when the system is partitioned and sends the first hard reset signal to the second domain when the system is not partitioned.

27. The system of claim 26, further comprising:

a third connection coupled between the first reset handler and both the first and second domains, wherein a power good signal is sent by the first reset handler over the third connection to both the first domain and the second domain irrespective of whether the system is partitioned or not.